

Application Serial No.: 09/655,352
Amendment under 37 C.F.R. § 1.114 being
filed concurrently with Request for
Continued Examination (RCE)

REMARKS

Claims 1-26 are pending in the present application, Claims 1-12 having been amended and Claims 13-26 having been added by way of the present Amendment.

The Notice of Allowance contained several objections to the drawings. More specifically, Figures 11-15 were objected to for not containing a legend such as "Prior Art." The Applicants have submitted concurrently herewith Replacement Sheets that include Figures 11-15 that have been amended to include the legend "Prior Art." Accordingly, the Applicants request the withdrawal of this objection to Figures 11-15.

Additionally, the drawings were objected to under 37 CFR 1.83(a). The Applicants respectfully traverse this objection. The Notice of Allowance indicates that a first time measurement circuit, a second time measurement circuit, and a velocity error signal generation circuit must be shown in the figures. The Applicants respectfully submit that these features are depicted in the figures of present application. For example, Figure 5 depicts a logical circuit chart showing one non-limiting example of a velocity error detection circuit (27) of Figure 2. The circuit (27) generates velocity error detections signals ACRRY and BCRRY, as depicted in Figure 5. (See page 29, lines 22-27.) Page 34, lines 1-19, describe how velocity error signals ACRRY and BCRRY are generated by the circuit (27) depicted in Figure 5. Accordingly, the Applicants submit that the figures depict an embodiment of a velocity error signal generating circuit. Furthermore, Figure 5 depicts a circuit (27) that includes FVACTR (51) that is a first velocity error detection counter and measures the moving velocity of the light beam after the generation of the normal direction

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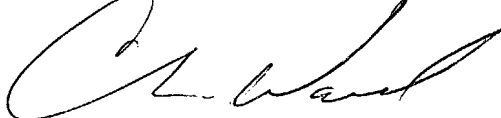
on-track signal, and FVACTR (52) that is a second counter and measures the moving velocity of the light beam after the generation of the normal direction off-track signal. (See page 30, line 24, through page 31, line 3.) FVACTR (51) and FVBCTR (52) are time measurement circuits each comprising a 5-bit counter. (See page 32, lines 4-11.) Accordingly, the Applicants submit that the figures depict a first time measurement circuit and a second time measurement circuit. Thus, the Applicants respectfully request the withdrawal of the objection to the drawings under 37 CFR 1.83(a).

Newly added Claims 13-26 are considered allowable as they recite features of the invention that are neither disclosed nor suggested by the references of record. No new matter has been entered.

It is respectfully submitted that the present application is in condition for formal allowance and an early and favorable consideration of the application is therefore requested.

Respectfully Submitted,

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